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THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

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Serial No. 09/896,395

Filed: June 29, 2001

For: Virtual PCI Device Apparatus and Method

Group Art: 2181

Examiner: not assigned

Commissioner of Patents
Box Missing Parts
Washington, D.C. 20231

PRELIMINARY AMENDMENT

RECEIVED

JAN 29 2002

Technology Center 2100

Dear Sir,

In response to the Notice to File Missing Parts mailed August 21, 2001, Applicant respectfully submits the enclosed Substitute Drawings, which re-label Figs. 1a, 1b, 6a, and 6b as 1A, 1B, 6A, and 6B, respectively. To maintain consistency in the application, Applicant also requests entry of the following amendment, which amends the specification to reflect the new figure numbers. A clean version of the amended paragraphs is shown on the following pages. A marked-up version of the amended paragraphs is shown in Appendix A.

A fee for a one month extension of time is included for the Substitute drawings. If this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Clean Version of Amended Paragraphs

At paragraph 7 on pages 3-4:

A1
Plug-and-Play TM resource allocation programs, as required by PCI bridge specifications, typically expect the address space allocated to a particular PCI bus to include the address space allocated to any PCI bus behind that particular PCI bus. Accordingly, full compliance with PCI protocol increases the difficulty of locating PCI devices on the host processor side of a host-to-PCI bridge, where the PCI devices - possibly for compatibility reasons - require an address space that may be a subset of the address space allocated to a physical PCI bus.

BRIEF DESCRIPTION OF DRAWINGS

Figs. 1A, 1B show a system configuration in accordance with the present invention.

Fig. 2 shows a more detailed system configuration.

Fig. 3 shows a system with a primary virtual bridge.

Fig. 4 shows a system with a secondary virtual bridge and a primary virtual bridge.

Fig. 5, 6A, 6B show flow charts of method embodiments.

At paragraph 9 on page 5:

A2
Figs. 1A, 1B, 2, 3 and 4 show block diagrams of systems 100, 200, 300 and 400 for explaining various embodiments of the present invention. Processor 130 may represent

A2
end
any one processor coupled to host bus 120. Alternatively processor 130 may represent two or more processors coupled to host bus 120.

At paragraph 19, page 9:

A3
Fig. 1A shows host bus device 110 coupled to host bus through interface 112, which is distinct from the host bus interface to processor 130. Fig. 1B shows an alternate configuration consistent with the methods of the present invention, where processor 130 and host bus device 110 are coupled to host bus 120 through an internal bus 113 and a shared host bus interface 112. The system of Fig. 1B can result from integrating host bus device 110 and processor 130 into a single circuit package.

At paragraph 39, page 17:

A4
Fig. 6A and 6B show flow diagrams for explaining a method 600 executed by monitor circuit 114 of system 400, which is shown in Fig. 4. Start (step 610) and capturing (step 620) may be the same as described for steps 510 and 520, respectively. Assessing (step 540) and snooping (step 560) are accomplished with steps 641, 642, 662 and 664. Likewise assessing step 550 and intercepting step 580 are accomplished with steps 643, 644, 645, 682, 684, and 686. Assessing steps 641-645 may take place substantially in parallel during the address phase of a host bus cycle, and if snooping step 662, 664 or intercepting step 682, 684, 686 is executed, then the snooping or intercepting step may take place during the data phase of a host bus cycle. Snooped cycles may be

A4 completed (e.g. terminated) by a device other than host bus device 410 and intercepted cycles may be completed by the host bus device 410.

Respectfully submitted,

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